FIG. 1 PRIOR ART

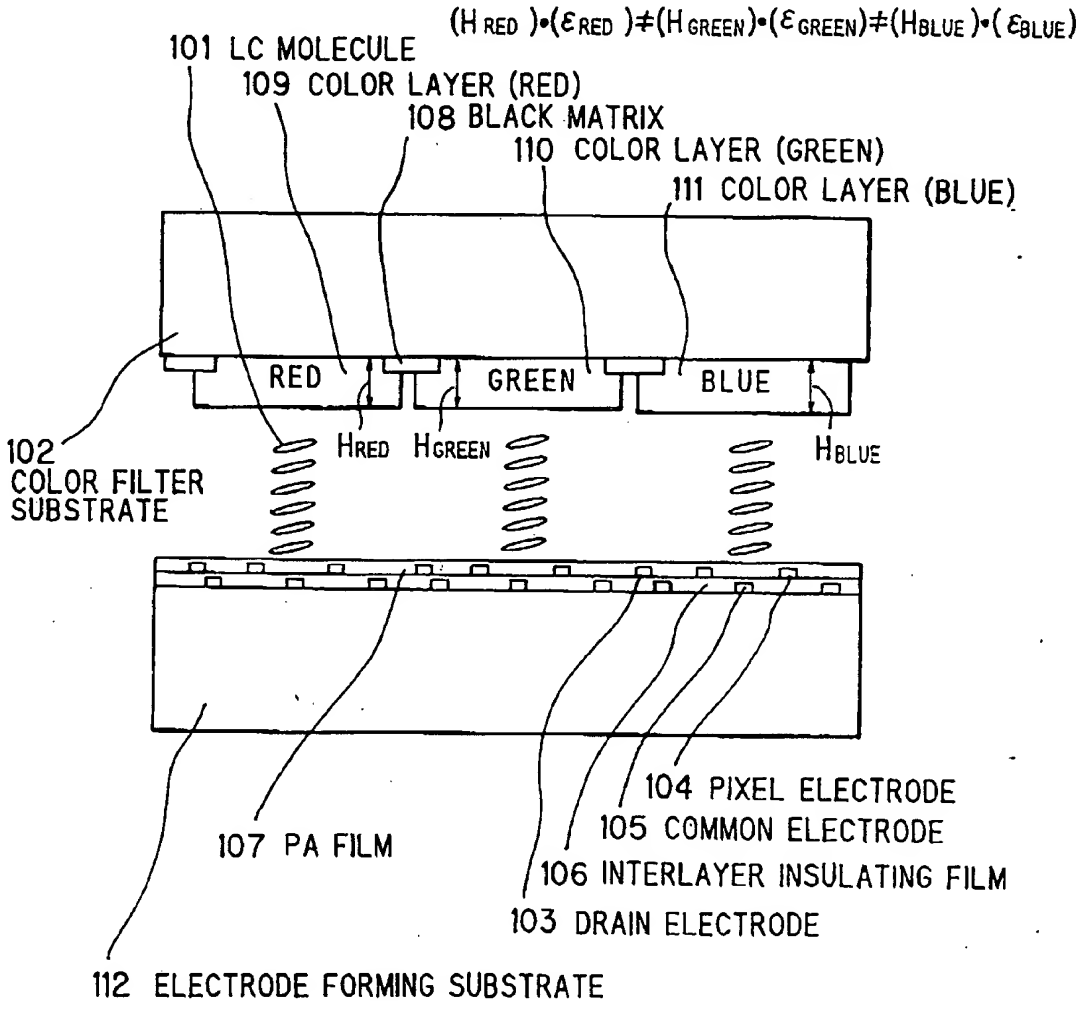


FIG.2 PRIOR ART

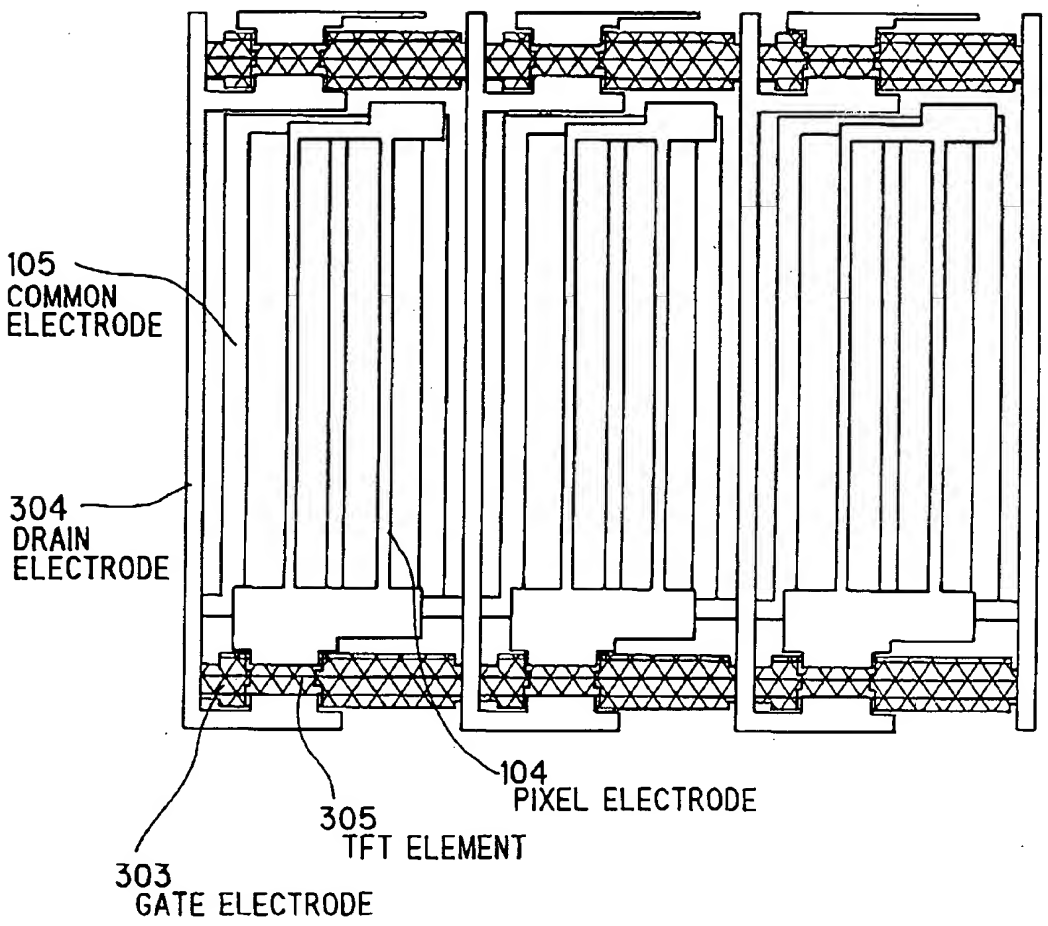
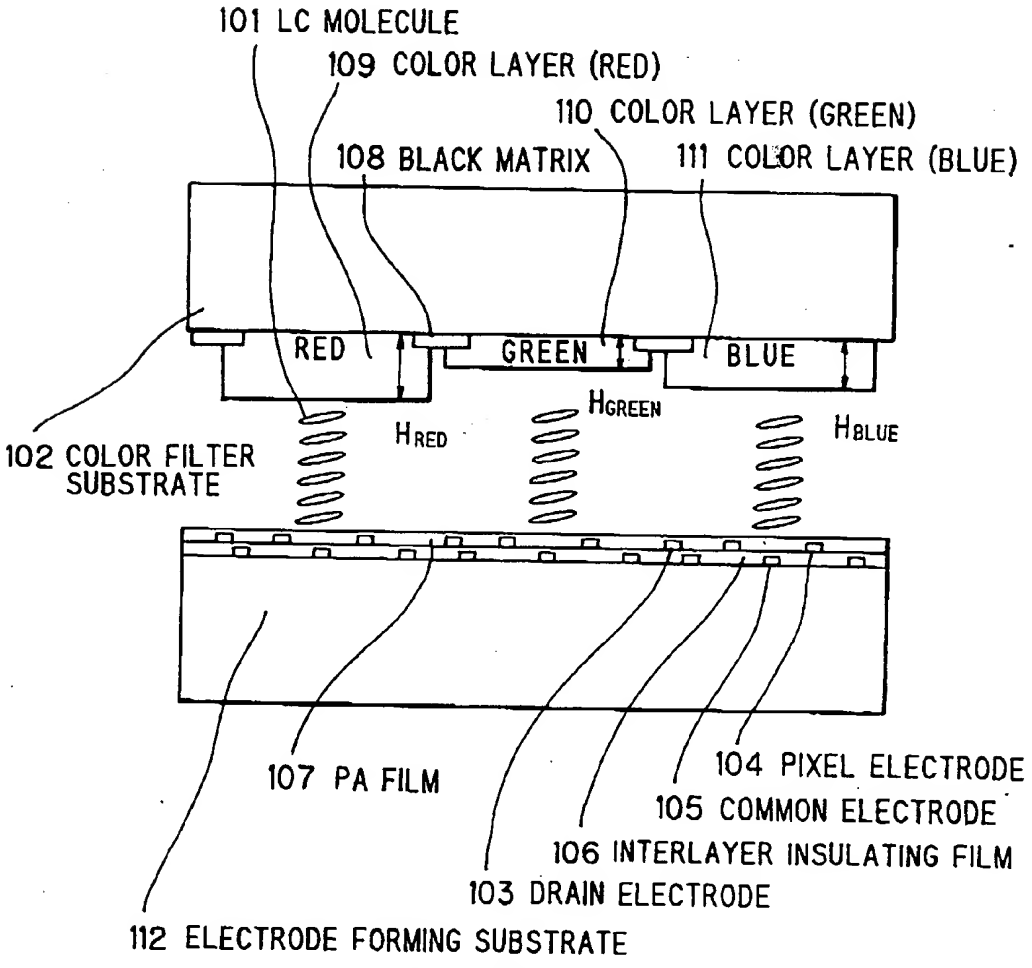


FIG.3



$$(H_{RED})\cdot(\varepsilon_{RED})=(H_{GREEN})\cdot(\varepsilon_{GREEN})=(H_{BLUE})\cdot(\varepsilon_{BLUE})$$

FIG.4

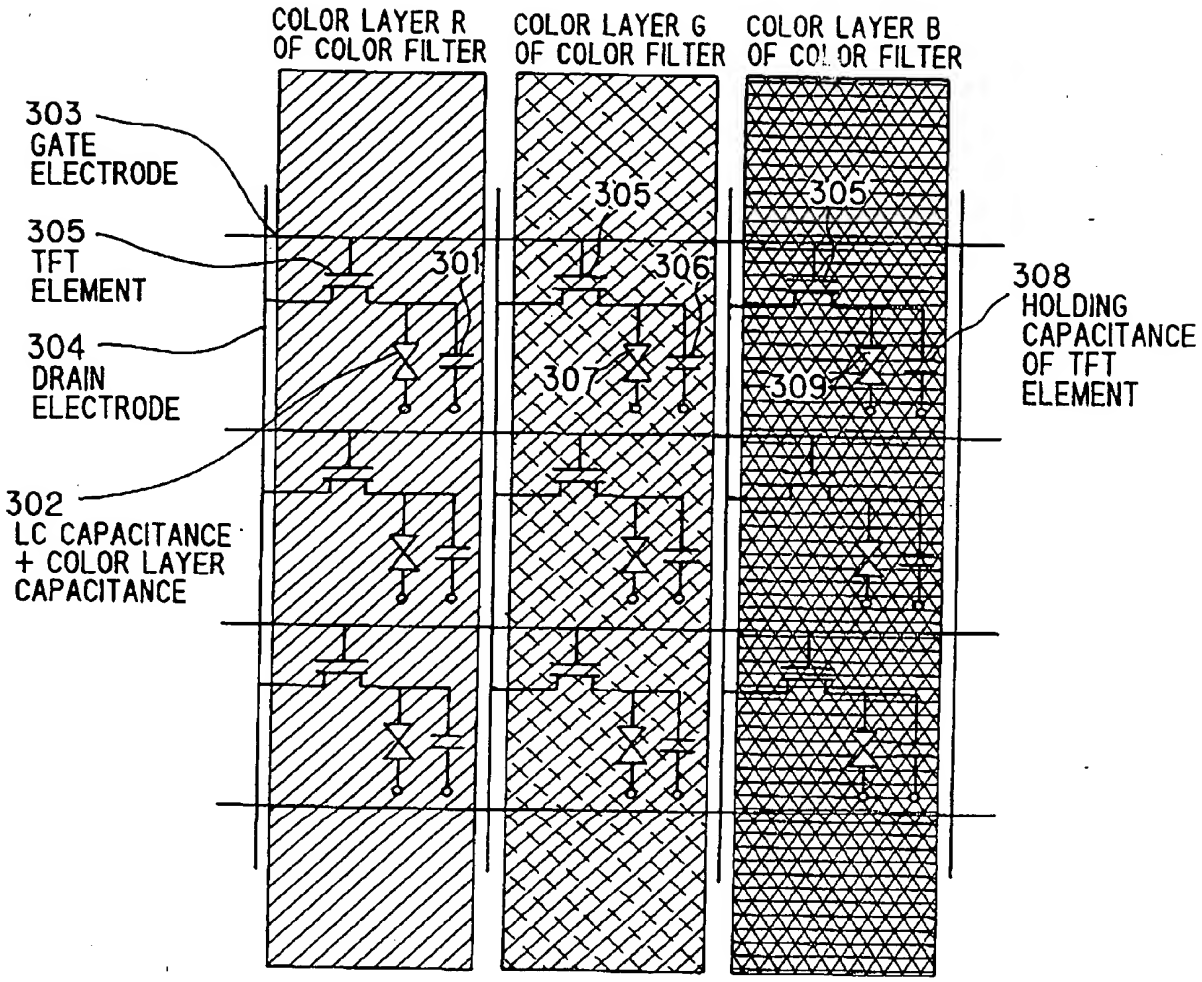

COLOR LAYER R OF COLOR FILTER
COLOR LAYER G OF COLOR FILTER
COLOR LAYER B OF COLOR FILTER
303 GATE ELECTRODE
305 TFT ELEMENT
304 DRAIN ELECTRODE
302 LC CAPACITANCE + COLOR LAYER CAPACITANCE
301
305
306
307
305
308 HOLDING CAPACITANCE OF TFT ELEMENT
309

FIG.5

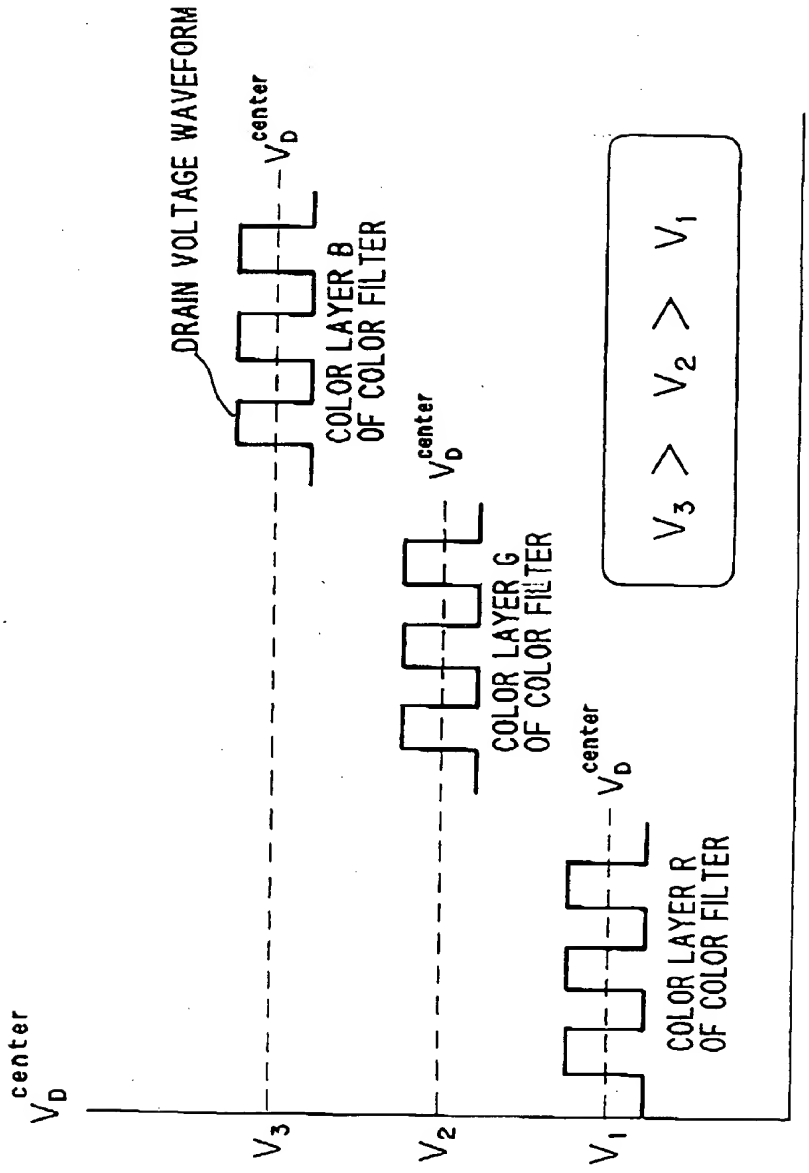

DRAIN VOLTAGE WAVEFORM
V_D^{center}
COLOR LAYER B OF COLOR FILTER
V_D^{center}
COLOR LAYER G OF COLOR FILTER
V_D^{center}
COLOR LAYER R OF COLOR FILTER
$V_3 > V_2 > V_1$
V_D^{center}
V_3
V_2
V_1

FIG.6

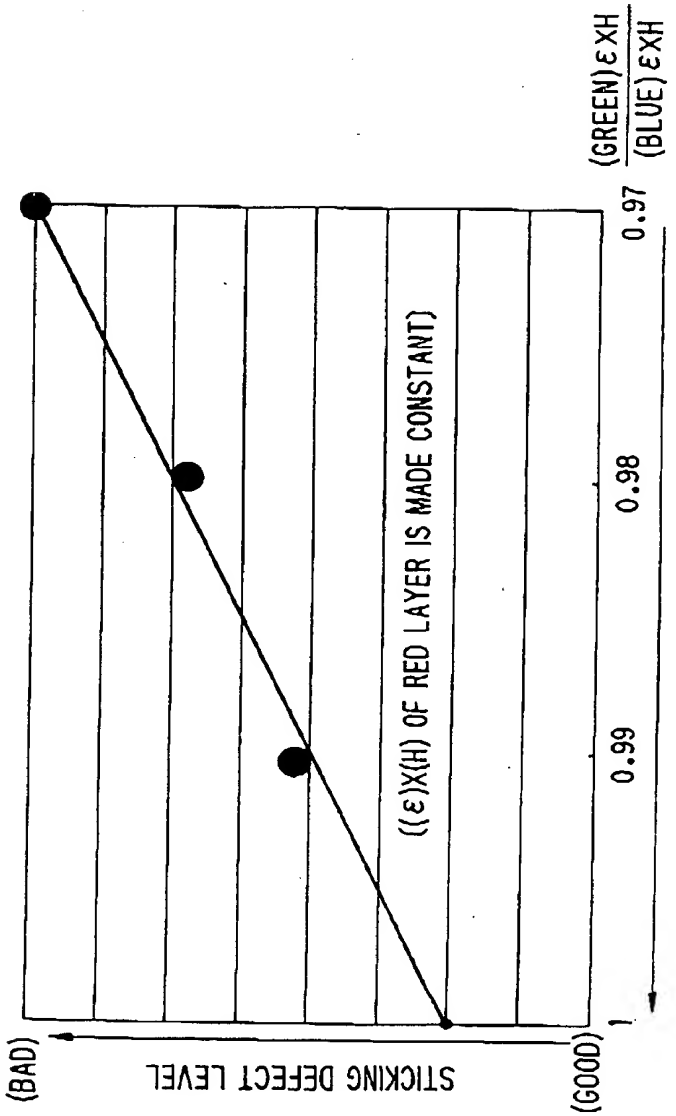

(BAD)
STICKING DEFECT LEVEL
(GOOD)
((ε)X(H) OF RED LAYER IS MADE CONSTANT)
0.99
0.98
0.97
(GREEN)εXH / (BLUE)εXH
DIRECTION WHERE "(COLOR-LAYER STATIC CAPACITANCE) + (LC STATIC CAPACITANCE)" OF RESPECTIVE COLOR LAYERS OF COLOR FILTER BECOMES EQUAL
(AT ABSCISSA POINT = 1, "(COLOR-LAYER STATIC CAPACITANCE) + (LC STATIC CAPACITANCE)" OF RESPECTIVE COLOR LAYERS ARE EQUAL)

FIG. 7

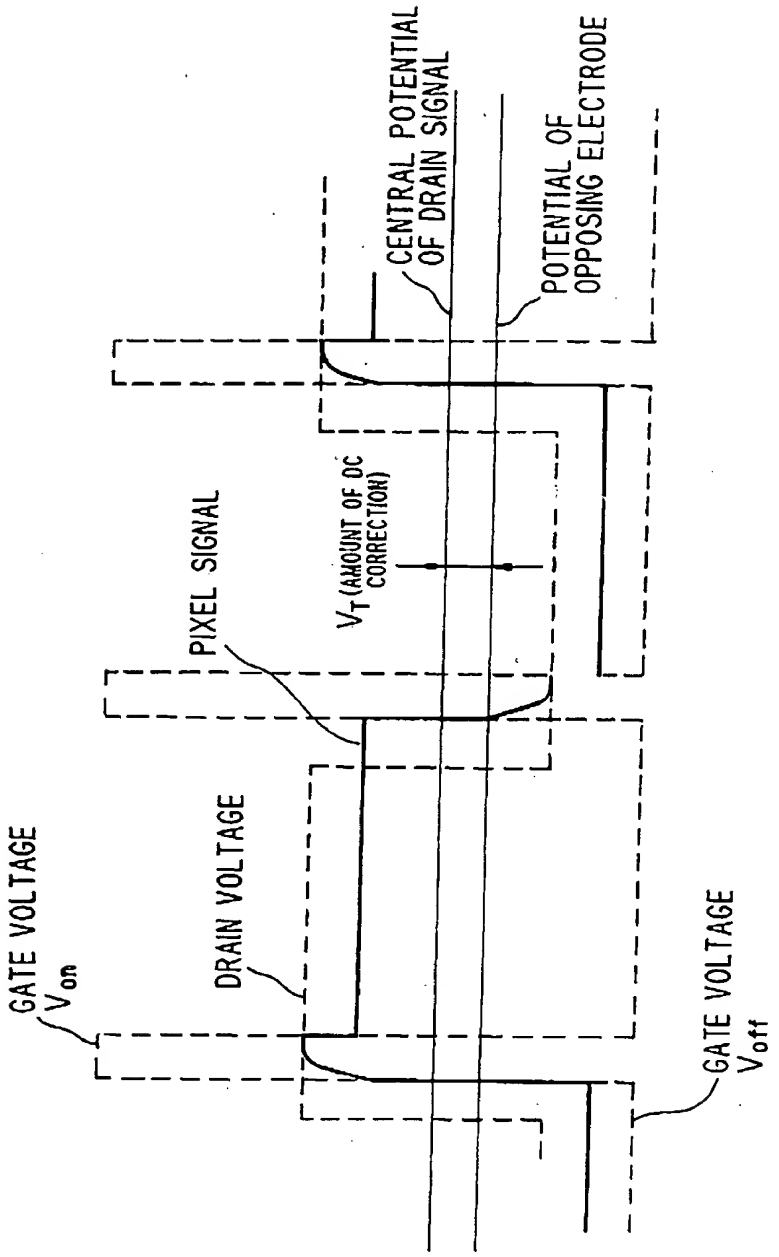
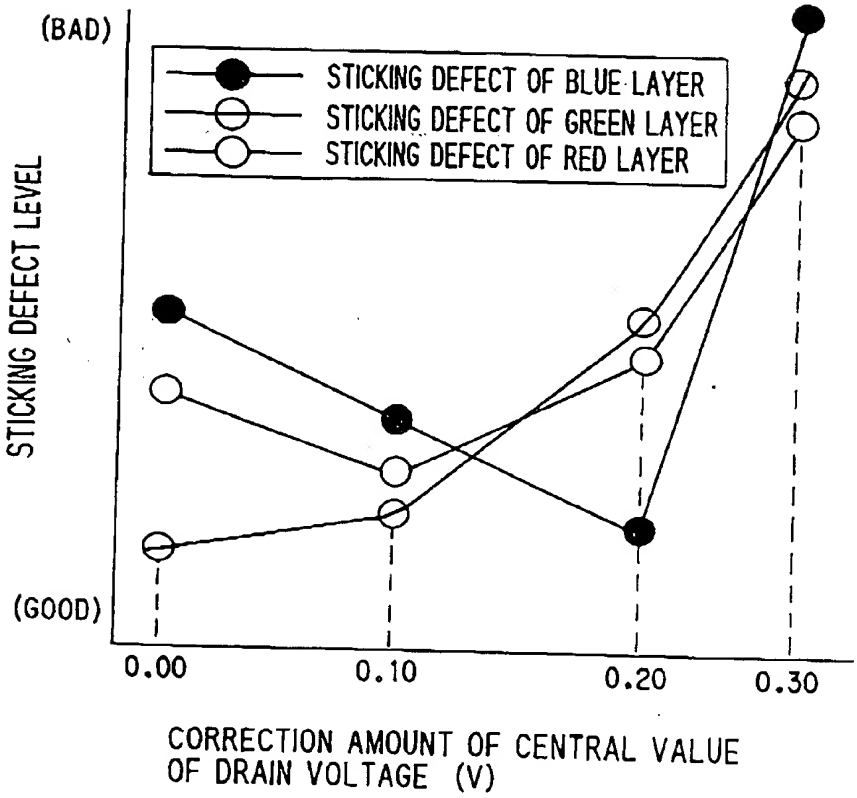

CENTRAL POTENTIAL OF DRAIN SIGNAL
POTENTIAL OF OPPOSING ELECTRODE
V_T (AMOUNT OF DC CORRECTION)
PIXEL SIGNAL
GATE VOLTAGE V_{on}
DRAIN VOLTAGE
GATE VOLTAGE V_{off}

FIG.8


(BAD)
(GOOD)
STICKING DEFECT LEVEL
STICKING DEFECT OF BLUE LAYER
STICKING DEFECT OF GREEN LAYER
STICKING DEFECT OF RED LAYER
0.00
0.10
0.20
0.30
CORRECTION AMOUNT OF CENTRAL VALUE
OF DRAIN VOLTAGE (V)